REMARKS

1. Objections to the drawings:

The drawings are objected to under 37 CFR 1.83(a).

1.1 The drawings must show every feature of the invention specified in the claims. Therefore, a plurality of layers, as recited in claim 3, must be shown or the feature(s) cancelled from the claim(s).

Response:

To overcome the drawing objection under 37 CFR 1.83(a) set forth on page 2 of the above detailed Office Action, a new figure, Fig.9, showing the implementation of the claimed invention in a multi-layer substrate, is submitted as an informal drawing for consideration. The basis for this new figure can be found in paragraph 0019 of the Detailed Description, specifically: "The inductor according to the present invention can be composed of multi-layered coils and can be manufactured by printed circuit board technology", and, "being isolated by a plurality of insulating layers". At this time, the specification has not been amended to include references to the new figure.

1.2 The drawings are objected to because trace 24 in figure 3 is not depicted as a thick line, and thus does not clearly illustrate that P4 is connected to P5.

Response:

To overcome the drawing objection under 37 CFR 1.83(a) set forth on page 2 of the above detailed Office Action, Fig.3 is resubmitted with informal amendments for consideration, care having been taken to ensure that all lines representing interconnection are suitably emboldened.

1.3 Figure 3 does not depict a connection between the first wiring [layer] 16 and P7

and between the second wiring [layer] 18 and P8.

Response:

The precise nature of this objection is not clear to the Applicant; P7 and P8 form the terminals of the inductor coil formed from the traces and vias disposed on the first and second wiring layers (16 & 18). Fig.3 shows P7 connected via a trace disposed on the first wiring layer 16 to the first clockwise via in the +Y direction. Similarly, P8 is shown connected via a trace disposed on the first wiring layer 16 to the first clockwise via in the -Y direction. The inductor terminals may be disposed on either wiring layer depending upon prevailing layout requirements, paragraph 0018 refers, specifically: "In order to comply with different layout requirements, the inductor 14 can be of varied forms".

Since P7 and P8 merely identify the ends of the traces, clarification or withdrawal of this objection is requested.

1.4 Figure 4 is not a clear sectional drawing along a cross-section 4-4' of the inductor 14 shown in figure 3, because traces 22 and 24 and vias 30 and 32 are all connected to each other, and because a perpendicular cut along cross-section 4-4' would not depict the entire length of trace 22, as shown in figure 4.

Response:

To overcome the drawing objection under 37 CFR 1.83(a) set forth on page 2 of the above detailed Office Action, Fig.4 is resubmitted with informal amendments for consideration, the cross-section line 4-4' of Fig.3 is also amended. As suggested, when viewed in section in the -Y direction, only trace 24 and vias 30 and 32 will lie in the indicated plane, hence trace 22 is mostly deleted, only its connection to via 30 is represented. Similar treatment is applied to the terminating end of trace 26.

1.5 Figures 5-8 depict traces 38 and 39 formed on wirings 16 and 18, being located on the same plane and connected to each other. Traces 38 and 39 cannot be located on

the same plane, because then wirings 16 and 18 are located on the same plane, and the disclosure recites wirings 16 and 18 being formed parallel to each other.

Response:

The Applicant respectfully points out that in the top-views of figures 5-8, trace 39 is shown as a broken line of the style generally used to depict 'hidden detail'. The applicant therefore asserts that trace 39 is depicted as being disposed on a separate layer to that on which trace 38 is disposed, as supported by paragraph 0018, lines 4-6: "In Fig.5 to Fig.8, conductive traces 38, shown as solid lines, are formed on the first wiring layer 16 and conductive traces 39, shown as broken lines, are formed on the second wiring layer 18".

Upon examiner's acceptance of the informal proposed corrections to the drawings, formal corrected drawings will be submitted.

2. Objections to the specification:

The disclosure is objected to because of the following informalities: Paragraph recites recite numerous grammatically incorrect terms such as "athe" and "andspiral".

Response:

The specification is amended in order to overcome the objection set forth on page 3 of the above detailed Office Action, in only being directed to "numerous" grammatical errors, the Applicant has taken the time to correct all obvious grammatical errors.

3. Claim rejections under 35 USC 112, second paragraph:

Claims 1-6 are rejected under 35 U.S.C. 112, the claimed limitations of first and second conductive traces formed on the first wiring and second wiring layers, as recited in claim 1, are unclear as to how first and second conductive traces can be

formed on the first wiring and second wiring layers without short circuiting the device.

Response:

Claims 1 and 3 are amended in order to overcome the rejections under 35 U.S.C. 112 set forth on page 4 of the above detailed Office Action.

In claim 1, further limiting terminology is included to recite the structure as being that of "a printed circuit board", the wiring layers of which are separated by "an insulating material". This additional structure provides the means for the respective layers to be formed without short-circuiting the device.

In claim 3, the clause containing the term alternately is replaced by more detailed recitation of the claimed invention structure, and seeks to clarify the disposition of the wiring layers, conductive traces and vias that constitute the inductive element.

3. Claim rejections under 35 USC 102:

Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Liou (6,037,649).

Response:

Claims 1 and 3 are further amended to recite that the vias directly connect the ends of the traces. No new matter is entered.

Liou's teachings are directed toward implementation of three dimensional inductive elements in integrated circuit technologies, whereas the claimed invention is directed toward realizing a three dimensional inductive element in a printed circuit board substrate, as supported by the limiting terminology included by amendment in claim 1, specifically: "a first wiring layer of a printed circuit board", and, "a second wiring layer of a printed circuit board".

Liou does not teach or suggest embodiments outside integrated circuit technology. Furthermore, Liou teaches the necessary intermediate second-level metal lines M2

requiring two vias (1st-level via 24 and 2nd-level via 27) per connection. The claimed invention as recited in amended claims 1 and 3 does not require such intermediate elements since, among other reasons, printed circuit board manufacturing techniques are significantly different from those used for semiconductors.

Reconsideration of claims 1-6 is hereby requested. Claims 2, and 4-6 are dependent on claims 1 and 3 and should be allowed if claims 1 and 3 are found allowable.

Sincerely,

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